Application Hints (Continued)

reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

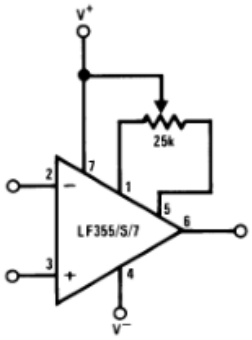
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pickup” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Circuit Connections

V_{OS} Adjustment



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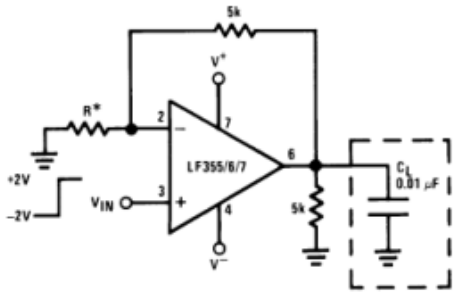
- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/˚C or less the additional drift with adjust is ≈ 0.5µV/˚C/mV of adjustment
- Typical overall drift: 5µV/˚C ±(0.5µV/˚C/mV of adj.)

Driving Capacitive Loads



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* LF155/6 R = 5k

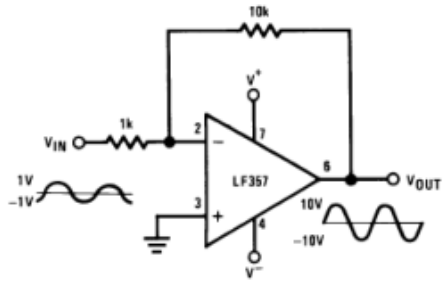
LF357 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)}$ = 0.01µF.

Overshoot ≤ 20%

Settling time (t_s) = 5µs

LF357. A Large Power BW Amplifier



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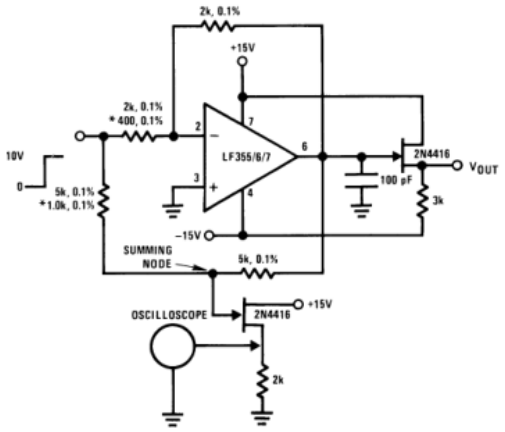
For distortion ≤ 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500kHz.

Typical Applications

Settling Time Test Circuit

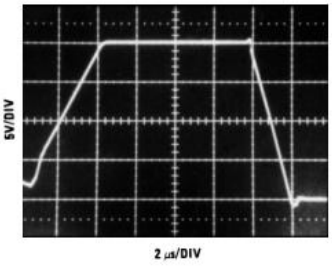


00564616

- Settling time is tested with the LF155/6 connected as unity gain inverter and LF357 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF357

Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)

LF355



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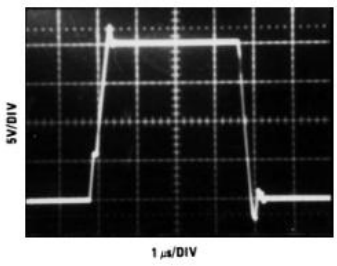
LF357



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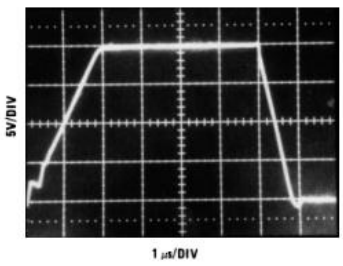
LF356



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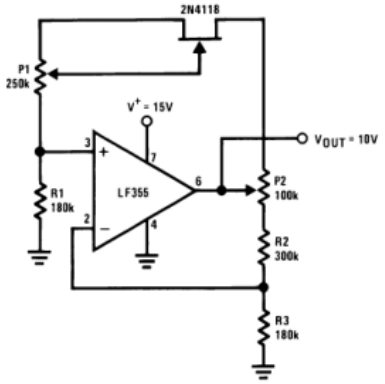
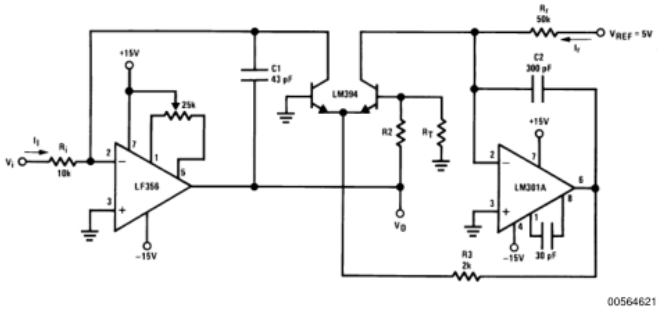
Low Drift Adjustable Voltage Reference



- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/^{\circ}C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - Low I_B
  - Low drift
  - Low supply current

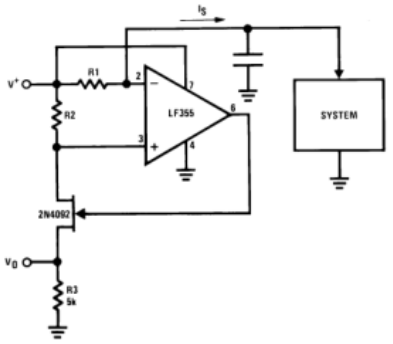
Fast Logarithmic Converter



- Dynamic range: $100\mu A \leq I_i \leq 1mA$ (5 decades), $|V_O| = 1V$/decade
- Transient response: 3µs for $\Delta I_i = 1$ decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \text{ in } V_i \left[\frac{R_r}{V_{REF}\ Ri}\right] = \log V_i \frac{1}{R_i I_r} \quad R2 = 15.7k,\ R_T = 1k,\ 0.3\%/^{\circ}C \text{ (for temperature compensation)}$$

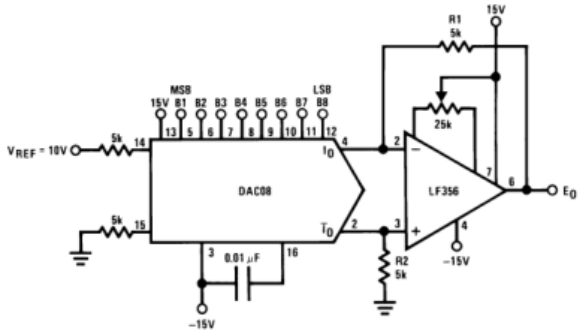
Precision Current Monitor



00564631

- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common-mode range to supply range
  - Low I_B
  - Low V_{OS}
  - Low Supply Current

8-Bit D/A Converter with Symmetrical Offset Binary Operation

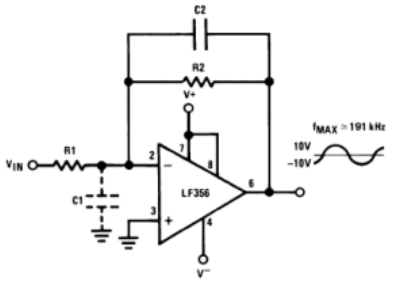


00564632

- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3μs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	Comments
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

Wide BW Low Noise, Low Drift Amplifier

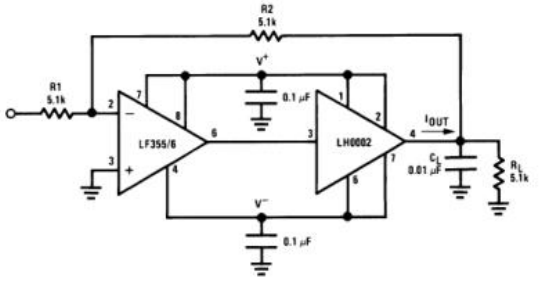


00564670

• Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 191\,kHz$

• Parasitic input capacitance C1 ≃ (3pF for LF155, LF156 and LF357 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2 C2 ≃ R1 C1.

Boosting the LF156 with a Current Amplifier



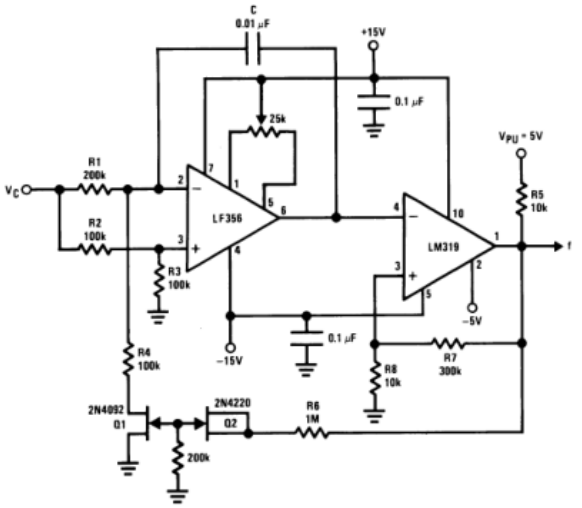
00564673

• $I_{OUT(MAX)} \simeq 150mA$ (will drive $R_L \geq 100\Omega$)

• $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}$ V/μs (with C_L shown)

• No additional phase shift added by the current amplifier

3 Decades VCO

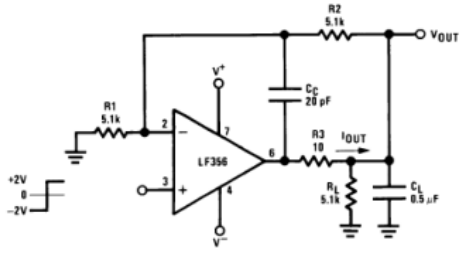


00564624

$$f = \frac{V_C\,(R8 + R7)}{(8\ V_{PU}\ R8\ R1)\ C'} \quad 0 \le V_C \le 30V,\ 10\,Hz \le f \le 10\,kHz$$

R1, R4 matched. Linearity 0.1% over 2 decades.

Isolating Large Capacitive Loads

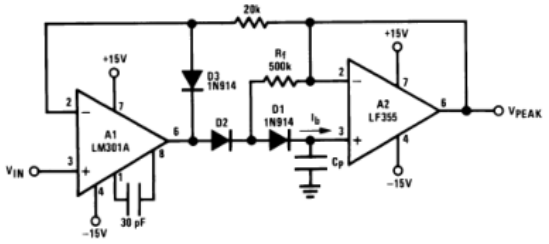


00564622

- Overshoot 6%
- t_s 10µs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s\ (\text{with } C_L \text{ shown})$$

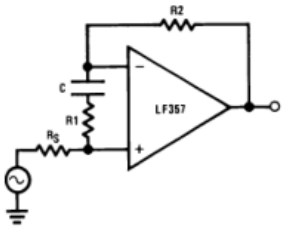
Low Drift Peak Detector



00564623

- By adding D1 and R_f, V_{D1}=0 during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of Cp.
- Diode D3 clamps V_{OUT} (A1) to V_{IN}–V_{D3} to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be << ½π$R_f C_{D2}$ where C_{D2} is the shunt capacitance of D2.

Non-Inverting Unity Gain Operation for LF157



00564675

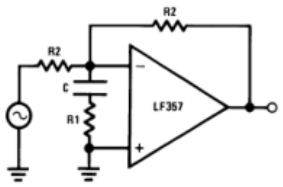
$$R1C \geq \frac{1}{(2\pi)\ (5\ MHz)}$$

$$R1 = \frac{R2 + R_S}{4}$$

$$A_{V(DC)} = 1$$

$$f_{-3\,dB} \approx 5\ MHz$$

Inverting Unity Gain for LF157



00564625

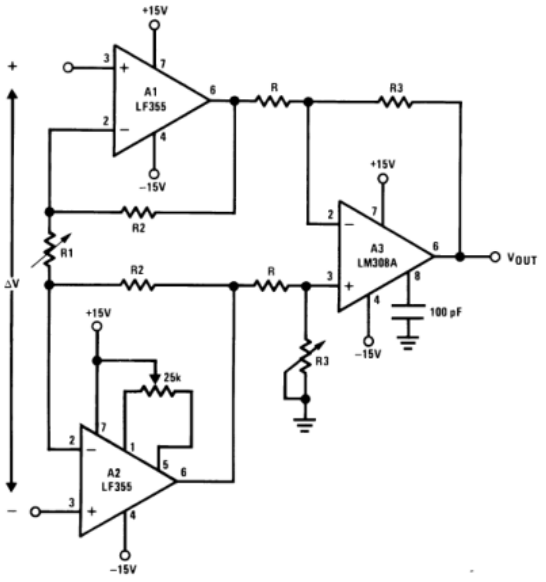
$$R1C \geq \frac{1}{(2\pi)\ (5\ MHz)}$$

$$R1 = \frac{R2}{4}$$

$$A_{V(DC)} = -1$$

$$f_{-3\,dB} \approx 5\ MHz$$

High Impedance, Low Drift Instrumentation Amplifier

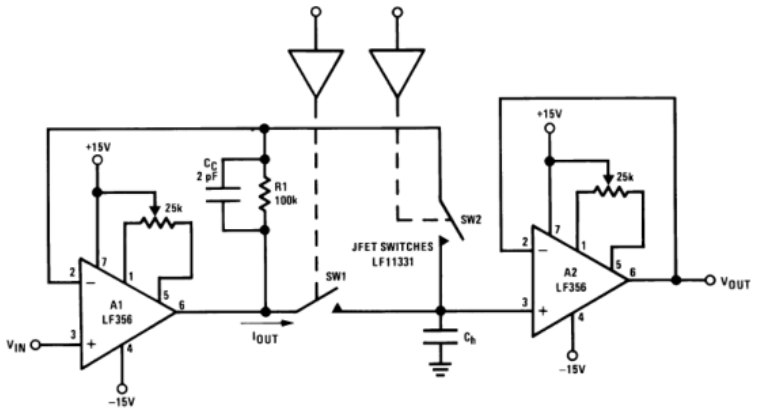


00564626

$$\bullet\ V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right]\Delta V,\ V^- + 2V \leq V_{IN}\ \text{common-mode} \leq V^+$$

- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

Fast Sample and Hold



00564633

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

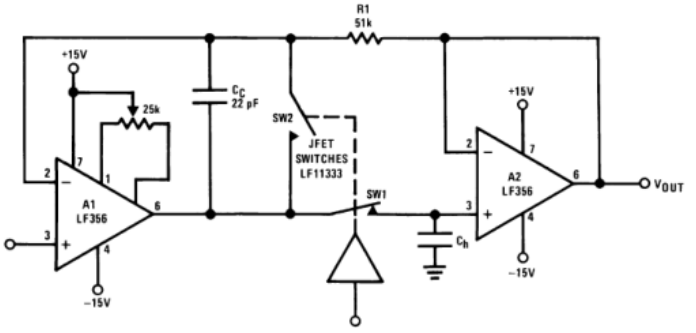
$$T_A \cong \left[\frac{2R_{ON},\ V_{IN},\ C_h}{S_r}\right] 1/2 \text{ provided that:}$$

$$V_{IN} < 2\pi S_r\, R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}},\ R_{ON} \text{ is of SW1}$$

$$\text{If inequality not satisfied: } T_A \cong \frac{V_{IN} C_h}{20\ mA}$$

- LF156 develops full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

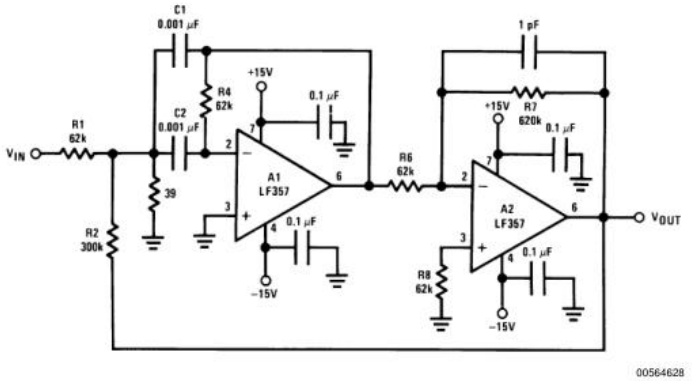
High Accuracy Sample and Hold



00564627

- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - Fast settling time
  - Low V_{OS}

High Q Band Pass Filter



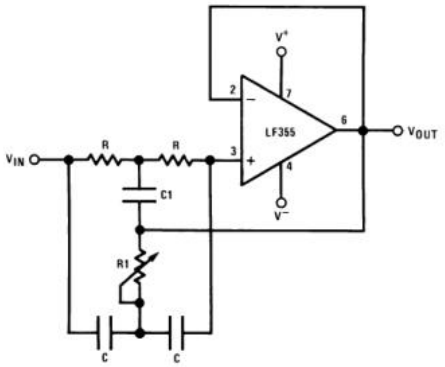
00564628

- By adding positive feedback (R2)
- Q increases to 40
- f_{BP} = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1Vp-p tone burst: 300µs

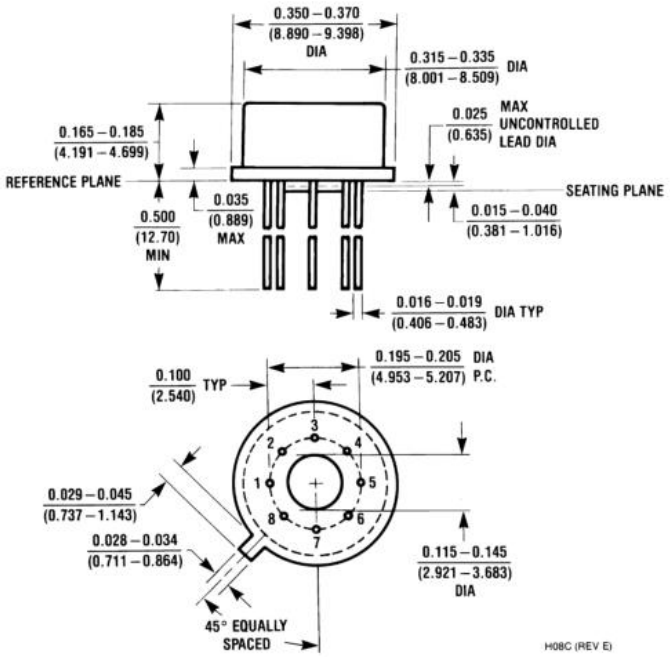
High Q Notch Filter



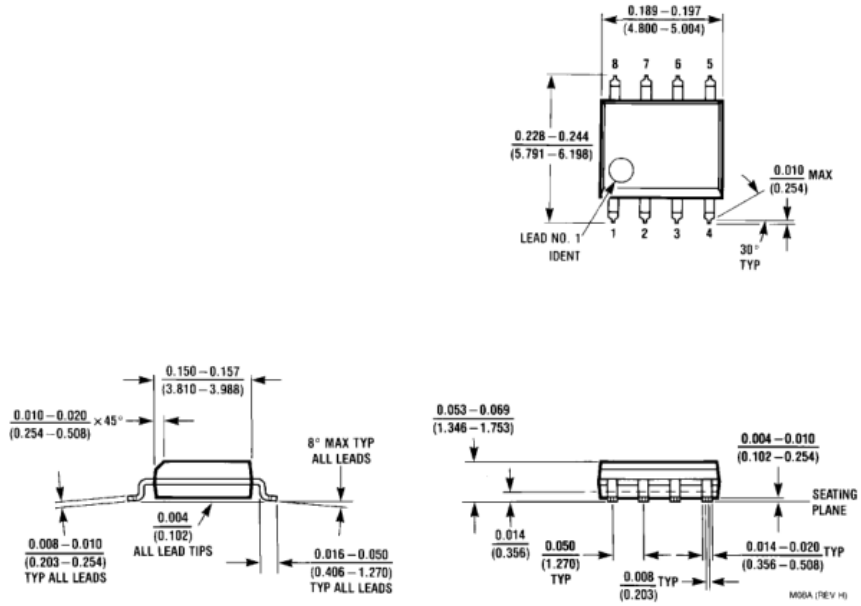
00564634

- 2R1 = R = 10MΩ
  2C = C1 = 300pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - Low I_B
  - Low supply current

Physical Dimensions inches (millimeters) unless otherwise noted

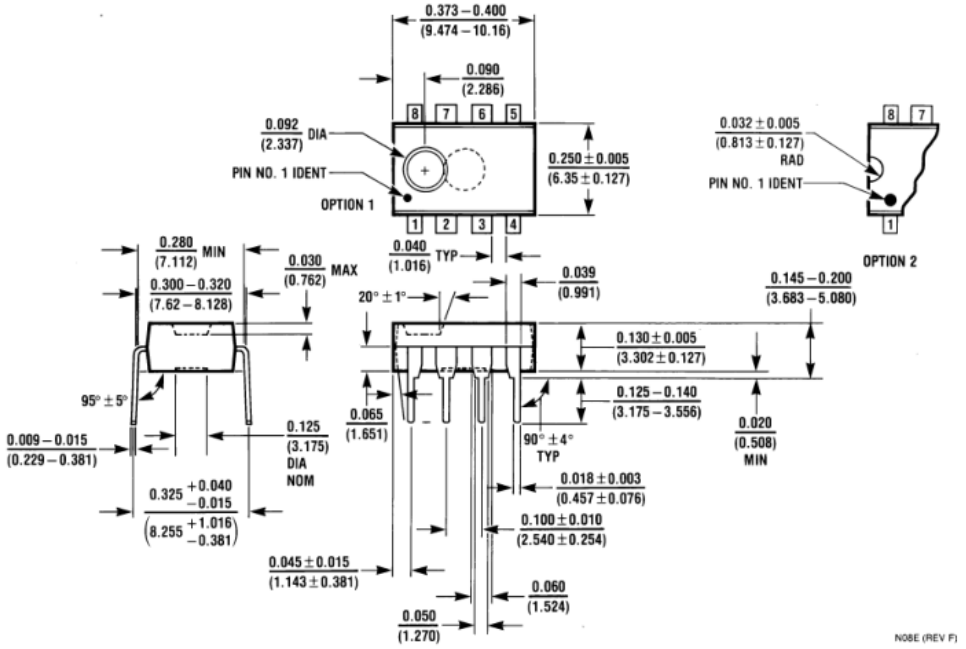


Metal Can Package (H)
Order Number LF155H, LF156H, LF256H, LF257H, LF356BH, LF356H or LF357H
NS Package Number H08C



Small Outline Package (M)
Order Number LF356M or LF356MX
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
Order Number LF356N
NS Package Number N08E