LF155/LF156/LF256/LF257/LF355/LF356/LF357 JFET Input Operational Amplifiers

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Features

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (5,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

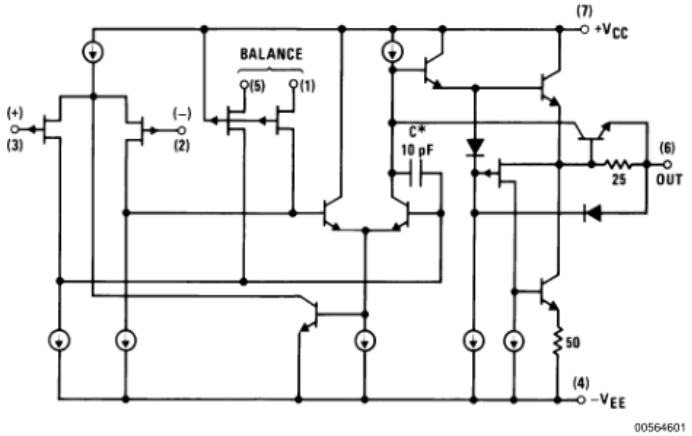
Common Features

- Low input bias current: 30pA
- Low Input Offset Current: 3pA
- High input impedance: $10^{12}\Omega$
- Low input noise current: $0.01\ pA/\sqrt{Hz}$
- High common-mode rejection ratio: 100 dB
- Large dc voltage gain: 106 dB

Uncommon Features

	LF155/ LF355	LF156/ LF256/ LF356	LF257/ LF357 (A_V=5)	Units
■ Extremely fast settling time to 0.01%	4	1.5	1.5	µs
■ Fast slew rate	5	12	50	V/µs
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	$nV/\sqrt{Hz}$

Simplified Schematic



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*3pF in LF357 series.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF155/6	LF256/7/LF356B	LF355/6/7
Supply Voltage	±22V	±22V	±18V
Differential Input Voltage	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous
T_{JMAX}			
H-Package	150˚C	115˚C	115˚C
N-Package		100˚C	100˚C
M-Package		100˚C	100˚C
Power Dissipation at T_A = 25˚C (Notes 1, 8)			
H-Package (Still Air)	560 mW	400 mW	400 mW
H-Package (400 LF/Min Air Flow)	1200 mW	1000 mW	1000 mW
N-Package		670 mW	670 mW
M-Package		380 mW	380 mW
Thermal Resistance (Typical) θ_{JA}			
H-Package (Still Air)	160˚C/W	160˚C/W	160˚C/W
H-Package (400 LF/Min Air Flow)	65˚C/W	65˚C/W	65˚C/W
N-Package		130˚C/W	130˚C/W
M-Package		195˚C/W	195˚C/W
(Typical) θ_{JC}			
H-Package	23˚C/W	23˚C/W	23˚C/W
Storage Temperature Range	−65˚C to +150˚C	−65˚C to +150˚C	−65˚C to +150˚C
Soldering Information (Lead Temp.)			
Metal Can Package			
Soldering (10 sec.)	300˚C	300˚C	300˚C
Dual-In-Line Package			
Soldering (10 sec.)	260˚C	260˚C	260˚C
Small Outline Package			
Vapor Phase (60 sec.)		215˚C	215˚C
Infrared (15 sec.)		220˚C	220˚C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance			
(100 pF discharged through 1.5kΩ)	1000V	1000V	1000V

DC Electrical Characteristics

(Note 3)

Symbol	Parameter	Conditions	LF155/6			LF256/7 LF356B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=50Ω, T_A=25˚C		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=50Ω		5			5			5		µV/˚C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	R_S=50Ω, (Note 4)		0.5			0.5			0.5		µV/˚C per mV
I_{OS}	Input Offset Current	T_J=25˚C, (Notes 3, 5)		3	20		3	20		3	50	pA
		$T_J \leq T_{HIGH}$			20			1			2	nA

DC Electrical Characteristics (Continued)

(Note 3)

Symbol	Parameter	Conditions	LF155/6			LF256/7 LF356B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_B	Input Bias Current	T_J=25˚C, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	T_J=25˚C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25˚C	50	200		50	200		25	200		V/mV
		V_O=±10V, R_L=2k										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k	±12	±13		±12	±13		±12	±13		V
		V_S=±15V, R_L=2k	±10	±12		±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15.1 −12		±11	±15.1 −12		+10	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics

$T_A = T_J = 25˚C$, $V_S = ±15V$

Parameter	LF155		LF355		LF156/256/257/356B		LF356		LF357		Units
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Supply Current	2	4	2	4	5	7	5	10	5	10	mA

AC Electrical Characteristics

$T_A = T_J = 25˚C$, $V_S = ±15V$

Symbol	Parameter	Conditions	LF155/355	LF156/256/ 356B	LF156/256/356/ LF356B	LF257/357	Units
			Typ	Min	Typ	Typ	
SR	Slew Rate	LF155/6: A_V=1,	5	7.5	12		V/µs
		LF357: A_V=5				50	V/µs
GBW	Gain Bandwidth Product		2.5		5	20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5	1.5	µs
e_n	Equivalent Input Noise Voltage	R_S=100Ω					
		f=100 Hz	25		15	15	$nV/\sqrt{Hz}$
		f=1000 Hz	20		12	12	$nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f=100 Hz	0.01		0.01	0.01	$pA/\sqrt{Hz}$
		f=1000 Hz	0.01		0.01	0.01	$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance		3		3	3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D=(T_{JMAX}-T_A)/\theta_{JA}$ or the 25˚C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

	LF155/156	LF256/257	LF356B	LF355/6/7
Supply Voltage, V_S	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \pm 20V$	$V_S = \pm 15V$
T_A	$-55^\circ C \le T_A \le +125^\circ C$	$-25^\circ C \le T_A \le +85^\circ C$	$0^\circ C \le T_A \le +70^\circ C$	$0^\circ C \le T_A \le +70^\circ C$
T_{HIGH}	$+125^\circ C$	$+85^\circ C$	$+70^\circ C$	$+70^\circ C$

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5µV/˚C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10˚C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta_{JA}$ Pd where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

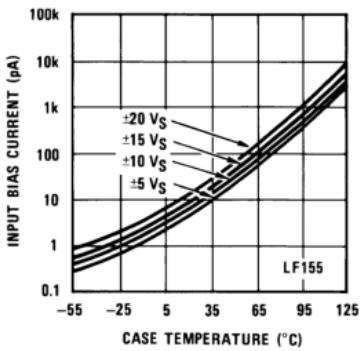
Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF357, $A_V = -5$, the feedback resistor from output to input is 2kΩ and the output step is 10V (See Settling Time Test Circuit).

Note 8: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical DC Performance Characteristics

Curves are for LF155 and LF156 unless otherwise specified.

Input Bias Current



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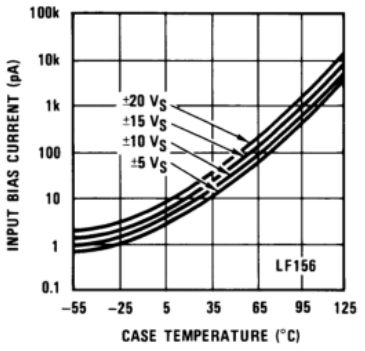
Input Bias Current



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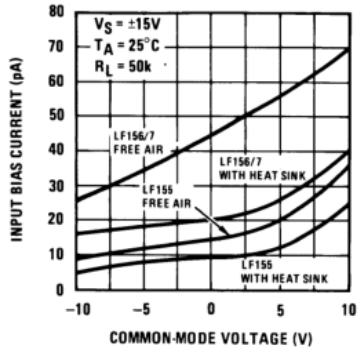
Input Bias Current



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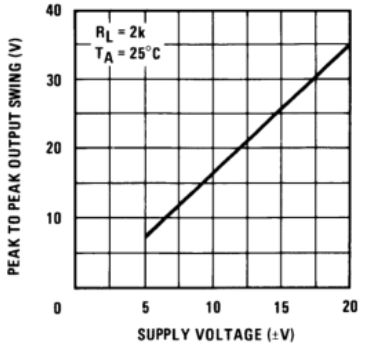
Voltage Swing



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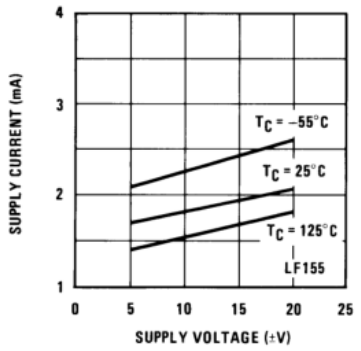
Typical DC Performance Characteristics

Curves are for LF155 and LF156 unless otherwise specified. (Continued)

Supply Current



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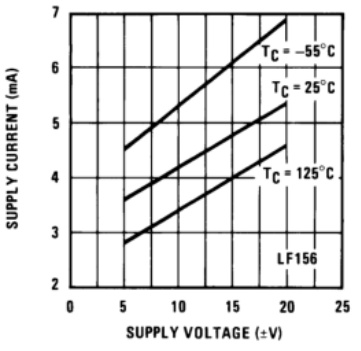
Supply Current



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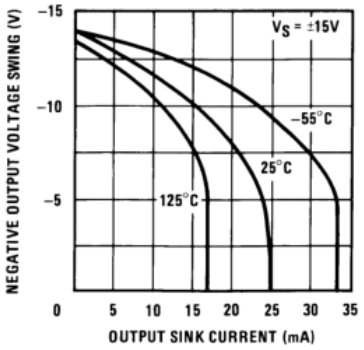
Negative Current Limit



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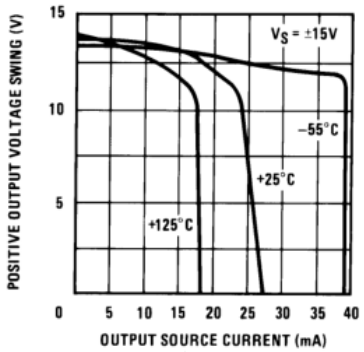
Positive Current Limit



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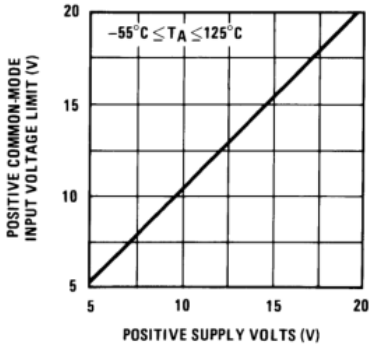
Positive Common-Mode Input Voltage Limit



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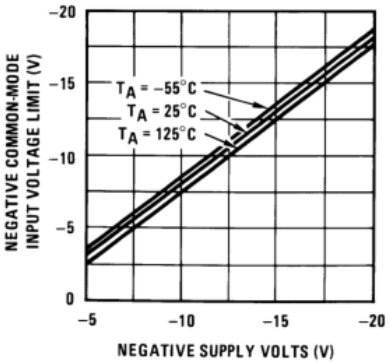
Negative Common-Mode Input Voltage Limit



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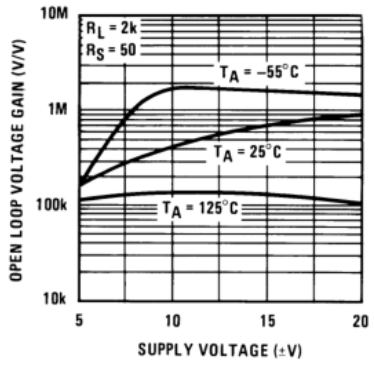
Typical DC Performance Characteristics Curves are for LF155 and LF156 unless otherwise specified. (Continued)

Open Loop Voltage Gain



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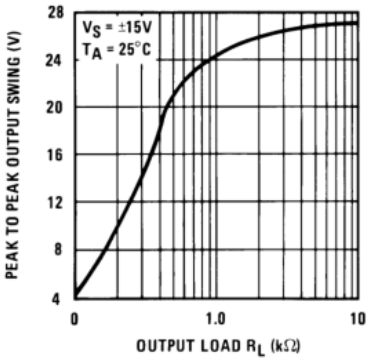
Output Voltage Swing



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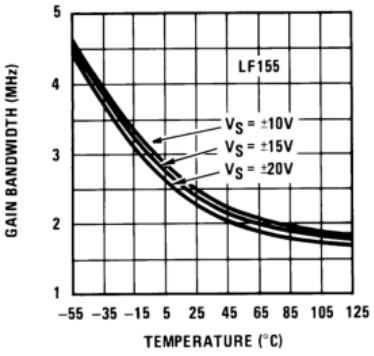
Typical AC Performance Characteristics

Gain Bandwidth



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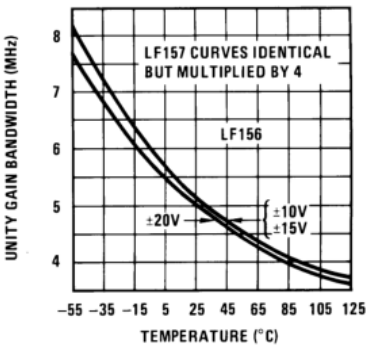
Gain Bandwidth



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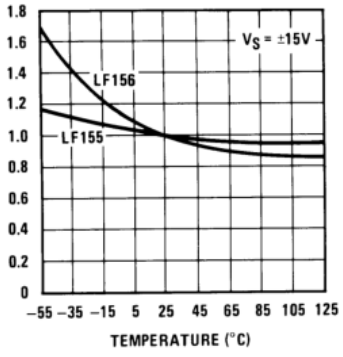
Normalized Slew Rate



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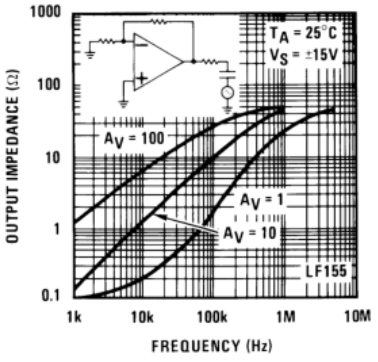
Output Impedance



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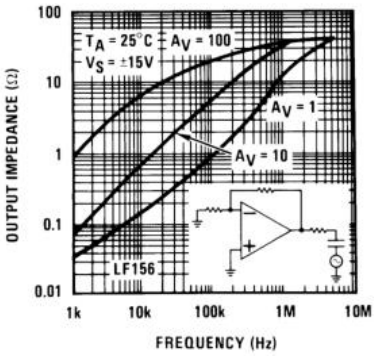
Typical AC Performance Characteristics (Continued)

Output Impedance



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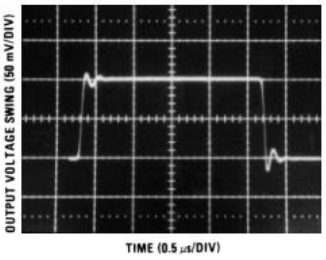
LF155 Small Signal Pulse Response, A_V = +1



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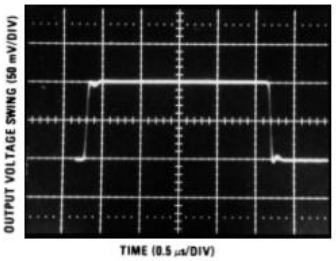
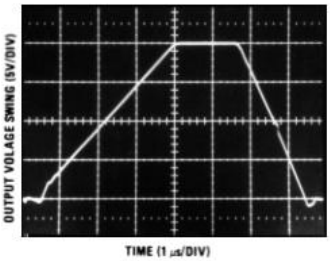
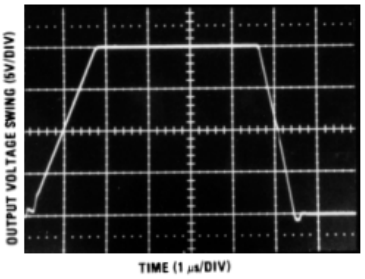
LF156 Small Signal Pulse Response, A_V = +1



LF155 Large Signal Pulse Response, A_V = +1



LF156 Large Signal Puls Response, A_V = +1



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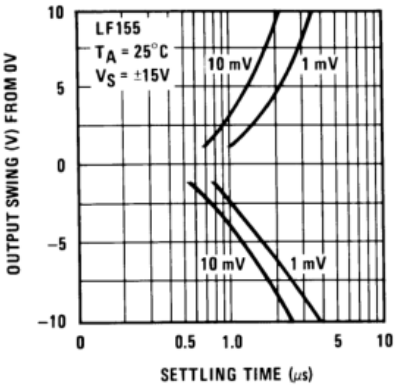
Inverter Settling Time



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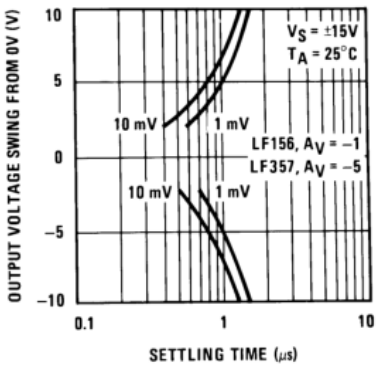
Typical AC Performance Characteristics (Continued)

Inverter Settling Time



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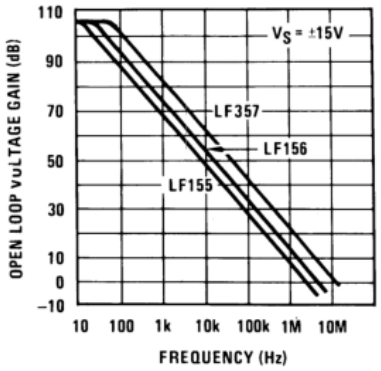
Open Loop Frequency Response



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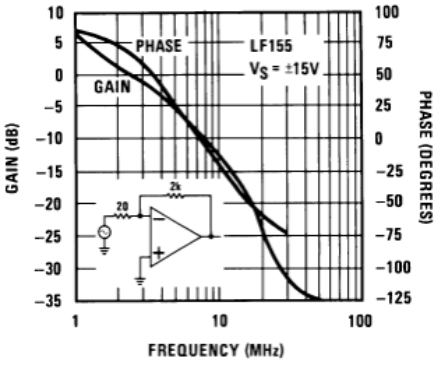
Bode Plot



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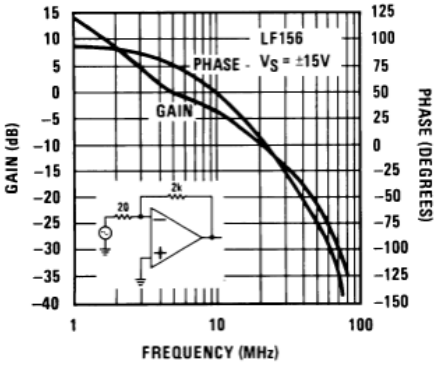
Bode Plot



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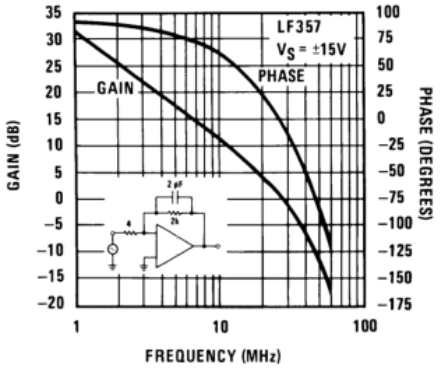
Bode Plot



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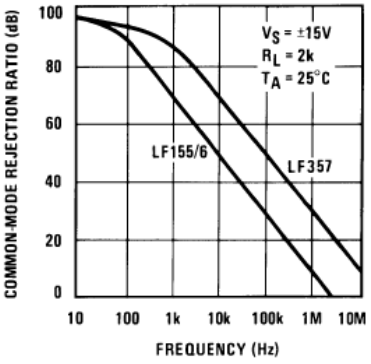
Common-Mode Rejection Ratio



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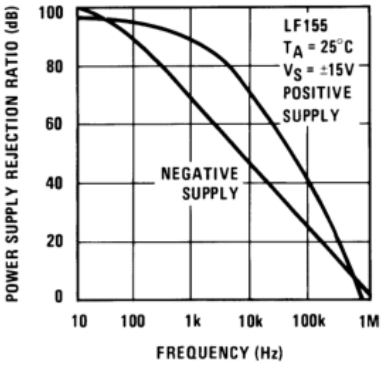
Typical AC Performance Characteristics (Continued)

Power Supply Rejection Ratio



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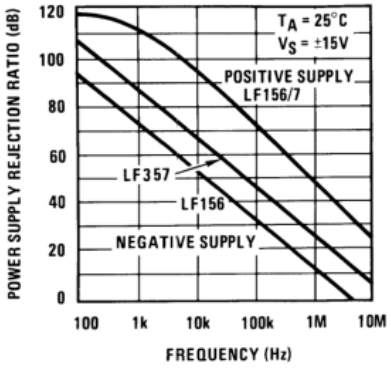
Power Supply Rejection Ratio



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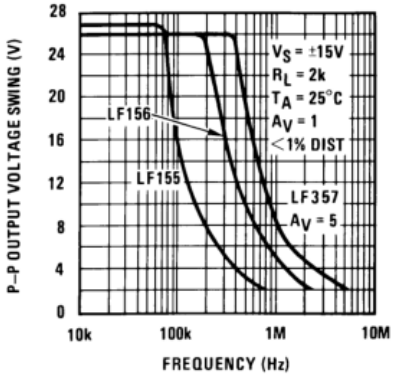
Undistorted Output Voltage Swing



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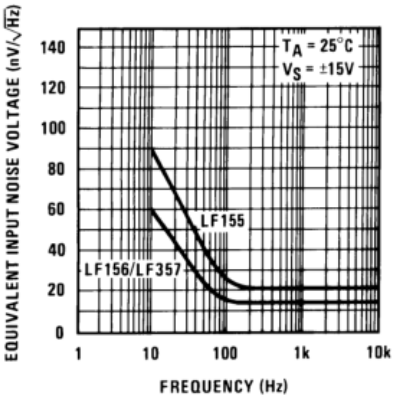
Equivalent Input Noise Voltage



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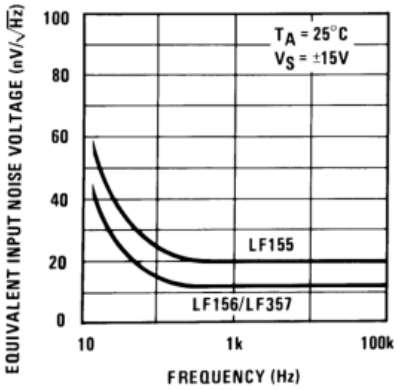
Equivalent Input Noise Voltage (Expanded Scale)



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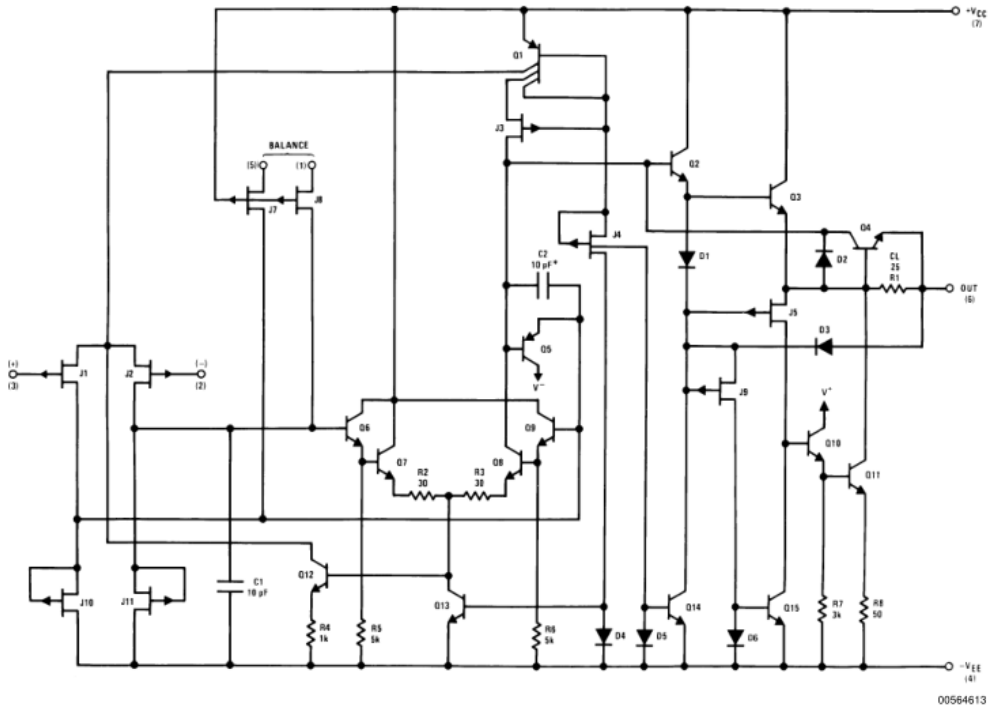
Detailed Schematic



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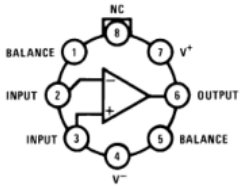
*C = 3pF in LF357 series.

Connection Diagrams (Top Views)

Metal Can Package (H)



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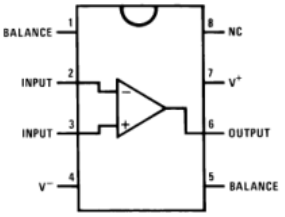
Order Number LF155H, LF156H, LF256H, LF257H, LF356BH, LF356H, or LF357H
See NS Package Number H08C

*Available per JM38510/11401 or JM38510/11402

Dual-In-Line Package (M and N)



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Order Number LF356M, LF356MX, LF355N, or LF356N
See NS Package Number M08A or N08E

Application Hints

These are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a